REMARKS

By this amendment, claims 1, 5, 11, 22, 34, and 35 have been amended and claims 36-38 have been added. Accordingly, claims 1-38 are pending in the present application. The claim amendments are new claims supported by the specification, the accompanying figures, and claims as originally filed, with no new matter being added. In particular, support for the amendments can be found at page 10, lines 6-21 of the application as filed. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

1. Rejection Under the Judicially Created Doctrine of Double Patenting

Claims 1-35 have been rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-32 of U.S. Patent No. 6,107,183 to Sandhu et al. (hereinafter "*Sandhu*") for the reasons set forth on page 4 of the Office Action.

This rejection will be addressed when allowable subject mater has been indicated by the Examiner.

2. Rejections Under 35 U.S.C. §103

Claims 1-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,445,996 to Kodera et al. (hereinafter "*Kodera*") in view of U.S. Patent No. 5,708,303 to Jeng (hereinafter "*Jeng* '303") and U.S. Patent No. 5,486,493 to Jeng (hereinafter "*Jeng* '493") for the reasons set forth on pages 2-4 of the Office Action. Applicants respectfully traverse.

In response, claim 1 has been amended to recite: "the layer of dielectric material extending above the upper surface of the adjacent lines of conductive material and below the lower surface of the lines of conductive material but not directly over or under the upper and lower surfaces of the

lines of conductive material." None of *Kodera*, *Jeng* '303, and *Jeng* '493 teaches or suggests this limitation. Claims 2-10 depend from claim 1 and include the limitations therein. Accordingly, claims 1-10 are not obvious in view of *Kodera*, *Jeng* '303, and *Jeng* '493 and Applicants therefore respectfully request that the rejection of claims 1-10 under 35 U.S.C. § 103(a) be withdrawn.

Claims 11-35 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kodera* in view of *Kodera*, *Jeng* '303, and *Jeng* '493 and U.S. Patent No. 5,641,382 to Shih et al. (hereinafter "*Shih*") for the reasons set forth on pages 4-6 of the Office Action. Applicants respectfully traverse.

Applicants respectfully submit that the rejection fails to give proper weight to the solution provided by the inventive method, the reduction of fringe capacitance. None of the cited references recognizes the need or provides a motivation to perform the recited methods. Therefore, in order to clarify the difference between the presently claimed invention, which addresses fringe capacitance, and the prior art, which does not, claims 11, 22, and 34 have been amended to recite some form of the limitation: "the layer of dielectric material extending above the upper surface of the lines of conductive material and below the lower surface of the lines of conductive material but not directly over or under the upper and lower surfaces of the lines of conductive material." Also, present claim 35 now recites: "wherein the dielectric material having a dielectric constant of less than about 3.6 extends both above and below, but not directly over, the respective adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween."

In contrast, Kodera does not teach a dielectric material layer extending below the bottom surface of a conductive layer, does not teach the use of low dielectric constant materials, does not address the problem of fringe capacitance, and in fact clearly illustrates a failure to comprehend, appreciate, or design for a solution to the problem of fringe capacitance. Rather, *Kodera* seeks to

improve a polishing operation on the upper surface of the dielectric layers 217, 246. In particular, *Kodera* uses a spacer layer to create a polishing stop. Although this creates a final product with a dielectric layer that extends higher than the adjacent conductor layer, this does not address the problem of fringe capacitance.

Similarly, neither of *Jeng* '303 or *Jeng* '493 teach or suggest the claimed methods of addressing the problem of fringe capacitance. Although both references acknowledge the need to reduce line-to-line capacitance and disclose the use of low dielectric constant dielectric materials, they do not teach or suggest extending a low dielectric constant dielectric layer above and below the upper and lower surfaces of adjacent conductive lines *to prevent fringe capacitance.* Hence, these references also provide no motivation to extend the dielectric layer.

Finally, *Shih* is cited for disclosing etching below the lower surface of adjacent conductive lines. However, Applicants respectively assert that *Shih* in fact expressly teaches away from any motivation to do so:

> [T]he etching time used to form the electrode pattern 15 can be increased to remove the silicon nodules but this will result in over etched regions 18 of the dielectric layer 12 and deterioration of the photoresist pattern 16 used to form the electrode pattern. The deterioration of the photoresist pattern can cause loss of photoresist at the pattern edge 17 resulting in a less desirable electrode cross section profile.

Shih at column 1, lines 57-64. Thus, while *Shih* acknowledges that is known to inadvertently overetch adjacent to conductive lines as part of the process to remove silicon nodules, the practice is clearly discouraged because of its associated problems of overetched regions of dielectric layers and loss of photoresist at the pattern edge.

Therefore, there would be no motivation to combine the teachings of *Jeng* '303 and *Jeng* *'493* regarding low dielectric constant dielectric materials with the teachings of *Shih*, which teaches

away from over-etching between adjacent conductive lines. Similarly, there is also no motivation to combine the polishing operation methods of *Kodera* (which result in a dielectric layer extending higher than adjacent conductive lines) with *Jeng* '303 and *Jeng '493* or with *Shih.*

Additionally, each independent claim now recites that the low dielectric constant layer does not extend directly over or under the upper and lower surface of the conductive lines. As disclosed in the application as filed, such a structure: "allows formation of contact holes such as contact hole 48 without exposing dielectric material 17 to processing agents that could degrade dielectric material 17 or upper surface 26 at contact hole 48." Specification at page 10, lines 19-21. The cited art does not teach or suggest this feature of the invention in combination with the other recited features of the invention.

Accordingly, Applicants therefore respectfully request that the rejection of the claims under 35 U.S.C. § 103(a) be withdrawn.

3. New Claims

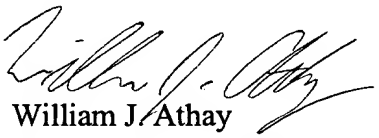
New claims 36-38 recite: "the layer of dielectric material having a dielectric constant of less than about 3.6 extends both above and below the respective adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween." Support for this limitation in the new claims can be found on page 10, lines 6-17 of the specification. As previously stated, there is no teaching or suggestion in the cited references of such a claimed feature. Accordingly, claims 36-38 also present patentable subject matter.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 4th day of September 2002.

Respectfully submitted,



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VERSION WITH MARKINGS SHOWING THE CHANGES MADE

In the claims:

1. (Once Amended) A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer, the conductive layer having an upper surface and a lower surface;

depositing an additional layer on said conductive layer;

patterning said conductive layer and said additional layer by:

forming a patterned mask layer on said additional layer;[,] and

etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the adjacent lines of conductive material and below the lower surface of the adjacent lines of conductive material but not directly over or under the upper and lower surfaces of the adjacent lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

5. (Once Amended) The method as defined in Claim 1, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

11. (Twice Amended) A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer, the conductive layer having a lower surface and an upper surface;

patterning said conductive layer by:

forming a mask layer on said conductive layer; and

etching through said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material each having an upper surface;

depositing an additional layer on the upper surfaces of lines of conductive material and on said first dielectric layer;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the lines of conductive material and below the lower surface of the lines of conductive material but not directly over or under the upper and lower surfaces of the lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

22. (Twice Amended) A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a metal layer on said first dielectric layer, the metal layer having a lower surface and an upper surface;

patterning said metal layer by:

forming a mask layer on said metal layer; and

etching through said metal layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said metal layer that extends below the lower surface of said metal layer, said adjacent remaining portions of said metal layer forming metal lines each having an upper surface;

depositing a thin layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the lines of conductive material and below the lower surface of the lines of conductive material but not directly over or under the upper and lower surfaces of the lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

34. (Twice Amended) A method of forming an interlevel dielectric comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer, the conductive layer having a lower surface and an upper surface;

forming an additional layer on said conductive layer;

forming lines of conductive material having spaces therebetween that extend below the lower surface of said conductive layer from the conductive layer;

filling the spaces between the lines of conductive material with dielectric material having a dielectric constant of less than about 3.6; and

forming a second dielectric layer on the additional layer;

wherein portions of the dielectric material having a dielectric constant of less than about 3.6 extend both above and below the adjacent lines of conductive material but do not extend directly over or under the upper and lower surfaces of the lines of conductive material.

35. (Twice Amended) A method of forming an interlevel dielectric that reduces fringe capacitance between adjacent lines of conductive material, the method comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer, the conductive layer having a lower surface;

forming an additional layer on said conductive layer;

etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

filling the spaces between adjacent remaining portions of said conductive layer with dielectric material having a dielectric constant of less than about 3.6; and

forming a second dielectric layer on the additional layer;

wherein the dielectric material having a dielectric constant of less than about 3.6 extends both above and below, but not directly over, the respective adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween.

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